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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,114	07/09/2003	Thomas Hanuschek	P2002,0587	2189

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EXAMINER	
TRUONG, LOAN	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,114	HANUSCHEK ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed June 15, 2006 in application 10/616,114.

2. Claims 1-8 are presented for examination. Claims 1, 5 and 6 have been amended. Claims 7 and 8 are newly added.

Response to Arguments

3. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajsuman et al. (US 6,249,893) in further view of Dahn (US 6,320,804).

In regard to claim 1, Rajsuman et al. teach an integrated module, comprising:

an external access terminal (*host computer, fig. 9, 61, col.8 lines 54-57)*;

a memory (*system memory, col. 4 lines 67)* including memory cells for storing code (*operand receives by the instruction execution unit, fig. 2, 14, col. 5 lines 5-7)* and data (*data, col. 5 lines 9-10)*;

a microcontroller (*basic structure of a microprocessor core, fig. 2, 10)* connected to said external access terminal (*host computer, fig. 9, 61, col.8 lines 54-57)* and to said memory (*program counter and instruction fetch unit, fig. 2, 12, col. 4 lines 64-65)*, said microcontroller (*basic structure of a microprocessor core, fig. 2, 10)* controlling an access (*operand or data for this computation are obtained from the system memory, col. 5 lines 9-10)* to said memory (*system memory, col. 4 lines 67)* and a data transfer (*multiplexer are used to switch the paths for these additional registers between the test mode and normal mode, col. 5 lines 26-28)* through said external access terminal during normal operation (*instruction and data flows during a normal mode, fig. 3, col. 5 lines 26-37)*, said microcontroller (*basic structure of a microprocessor core, fig. 2, 10)* controlling a performance of a test sequence (*microprocessor core generates a test pattern from the object code to applied to the memory core, fig. 9, col. 9 lines 2-12)* for functional testing (*read/write operation, col. 9 lines 13-18)* said memory in a test operation of the module (*TCR, LFSR, multiplexers, fig. 3, 22, 24, 32, 34, col. 5 lines 52-54)*; and

a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing.

Rajsuman et al. mention that the user can modify the test program to collect any desired test information of the embedded memory *(col. 9 lines 25-28)* but does not explicitly teach the storing addresses of the memory cells of said memory which have been detected as defective.

Dahn disclosed the memory unit for storing addresses of defective memory cells *(fig. 2, 10, col. 5 lines 6-15).*

It would have been obvious to modify the module of Rajsuman et al. by adding Dahn memory unit for storing addresses of defective memory cells. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would have considerable time advantage in the subsequent redundancy analysis *(col. 3 lines 34-41).*

In regard to claim 2, Rajsuman et al. disclosed the integrated module according to claim 1, further comprising a command memory *(test control register, fig. 3, 22, col. 5 lines 15-17)* for storing an externally *(test instruction is provide to the TCR through the controller, fig. 3, 28, col. 5 lines 54-56)* supplied command sequence *(provide opcode of microprocessor's instruction during the test mode, fig. 3, 22, col. 5 lines 15-17)* and on a basis of the command sequence *(microprocessor core generates a test pattern from the object code to applied to the memory core, fig. 9, col. 9 lines 2-12)* said microcontroller *(basic structure of a microprocessor core, fig. 2, 10)* controls a carrying out of the test sequence *(sequence of testing operation, fig. 10A, fig.*

11)..

In regard to claim 3, Rajsuman et al. does not explicitly teach the integrated module according to claim 1, wherein said defect data memory is part of said microcontroller.

Dahn disclosed the memory unit for storing addresses of defective memory cells *(fig. 2, 10, col. 5 lines 6-15)*. The memory unit may be located inside the semiconductor device (*col. 5 lines 14-15).*

Refer to claim 1 for motivational statement.

In regard to claim 4, Rajsuman et al. disclosed the integrated module according to claim 2, wherein said command memory is part of said microcontroller (*test control register (TCR) to provide opcode of microcontroller instructions during the test mode, fig. 3, 22, col. 5 lines 15-17).*

In regard to claim 5, Rajsuman et al. disclosed a method for functionally checking a memory of an integrated module, which comprises the steps of:

reading-in a command sequence externally before beginning a test operation (*host computer provide executable code of assembly language test program to the microprocessor core in the Soc chip through the I/O interface, fig. 9, 1, col. 8 lines 57-60)*, and on a basis of the command sequence a microcontroller controls a carrying out of a test sequence (*microprocessor core generates a test pattern from the object code and applied to the memory core, fig. 9, 10, 3, col. 9 lines 2-4)*;

executing the command sequence for carrying out the test sequence by the microcontroller (*test patterns are applied to the memory core by the microprocessor core, fig. 9, col. 9 lines 3-4)*; and

Rajsuman et al. mention that the user can modify the test program to collect any desired test information of the embedded memory (*col. 9 lines 25-28)* but does not explicitly teach the storing addresses of memory cells of the memory which have been detected as defective during the functional testing in a defect data memory under the control of the microcontroller.

Dahn disclosed the memory unit for storing addresses of defective memory cells (*fig. 2, 10, col. 5 lines 6-15).*

Refer to claim 1 for motivational statement.

In regard to claim 6, Rajsuman et al. disclosed the method according to claim 5, which further comprises:

making a jump to a start address in an internal command memory (*/*Test Procedure*/, move D0, [A0], fig. 10A)* after the command sequence is read-in at the beginning of the test operation (*/*Initialization, fig. 10A)*;

executing the command sequence under the control of the microcontroller proceeding from the start address (*/*Write/Read in increasing order*/, fig. 10A)*; and

Rajsuman et al. mention that the user can modify the test program to collect any desired test information of the embedded memory (*col. 9 lines 25-28)* and also the limitation of reading-out to outside the integrated module for further evaluation by having

the microprocessor core sends pass/fail signal to host computer via interface circuit (*fig. 11, col.9 lines 54-56)* but does not explicitly teach the storing the addresses of the memory cells of the memory which have been detected as defective during functional testing generated in the defect data memory under the control of the microcontroller; and reading-out the addresses of the memory cells of the memory which have been detected as defective during functional testing stored in the defect data memory, under the control of the microcontroller, to outside the integrated module for further evaluation.

Dahn disclosed the memory unit for storing addresses of defective memory cells *(fig. 2, 10, col. 5 lines 6-15)* and the memory unit and the preprocessing device are respectively fed addresses ADR of defective memory cells MC via an address bus (*fig. 2, 2, 3, col. 4 lines 47-50).*

Refer to claim 1 for motivational statement.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rajsuman et al. (US 6,249,893) in further view of Dahn (US 6,320,804) in further view of Suzuki et al. (US 2002/0066056).

In regard to claim 7, Rajsuman et al. and Dahn does not teach integrated module according to claim 1, wherein said defect data memory and said command memory are part of a dual-port RAM.

Suzuki et al. disclosed the method of testing semiconductor memory by having a dual-port RAM with one port for suppling data while the other port supplied with feedback data from data operation *(fig. 5, paragraph 0062)*.

It would have been obvious to modify the module of Rajsuman et al. and Dahn by adding Suzuki et al. method of testing semiconductor memory by having a dual-port RAM. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide optimum data for detecting a defect difficult to be detected by the regular test pattern *(paragraph 0064)*.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rajsuman et al. (US 6,249,893) in further view of Dahn (US 6,320,804) in further view of Saliba (US 5,894,425).

In regard to claim 8, Rajsuman et al. and Dahn does not teach the integrated module according to claim 1, wherein the microcontroller is embodied as a hard disk controller.

Saliba disclosed the method of a wireless secondary interface for data storage device where embedded controller technology have enabled computer mass storage devices having embedded controllers to include self-contained test, adaptation, upgrade and diagnostics capabilities *(col. 1 lines 14-17)*.

It would have been obvious to modify the module of Rajsuman et al. and Dahn by adding Saliba method of embedded controller technology. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the

modification because it would minimize handling of hard disk drives after installation into a computer in order to minimize damage (*col. 1 lines 40-42).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LOAN TRUONG whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SCOTT BADERMAN can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
Art Unit: 2114

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER